## **Claims**

What is claimed is:

1. A method of designing a clock tree in an integrated circuit comprising the steps of:

collecting a set of sink locations 3 in a master list and a set of blocked areas 47;

- (a) selecting a temporary insertion point (TIP) 4, 5;
- (b) enclosing the sink 41 at the first level furthest from the TIP in a bin 40 that includes a first subset of sinks 43 and remove the first subset from the master list;
- (c) assigning a first-level structured clock buffer (SCB) 42 to the bin;

repeating steps (a), (b) and (c) above for the remaining sinks in the first level of buffers and subsequent levels until the root level is reached;

improving the symmetry of the tree by moving SCB 45 locations within constraints 46 to concentrate SCBs in rows and columns;

connecting the root level TIP 610 to lower levels; and

connecting a source (S) of clock signals to the root level TIP.

2. A method according to claim 1, in which said step (a) of selecting a TIP (4,5) comprises calculating a center 4 of sinks and a centroid 5 of sinks and automatically placing said TIP at one of said center, centroid or an

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intermediate point between said center and centroid in accordance with an algorithm that locates available space.

- 3. A method according to claim 2, in which said step (a) of selecting a TIP (4,5) comprises calculating a center 4 of sinks and a centroid 5 of sinks and automatically placing said TIP at one of said center 4, centroid 5 or an intermediate point between said center and centroid in accordance with an algorithm that locates selectively weights one or more of delay, power consumed and placability.
- 4. A method according to claim 1, in which said step (c) of assigning a first-level SCB 42 to the bin comprises steps of attempting to place a horizontal SCB 42, then attempting to place a vertical SCB 42 in a central location when a horizontal SCB will not fit in said central location.
- 5. A method according to claim 4, in which said vertical SCB comprises a set of circuit elements laid out to have substantially the same delay as a corresponding SCB with horizontal layout.
- 6. A method according to claim 1, in which said step of improving symmetry comprises a step of calculating for each of a set of columns and rows a potential improvement in symmetry of SCBs 45 in an nth level of said tree and moving SCBs 45 to improve symmetry.
- 7. A method according to claim 6, in which some designated SCBs 142 are excluded from the calculation in said step of improving symmetry, whereby only a subset 45 of SCBs are included in the calculation.
- 8. A method according to claim 6, in which the amount of movement permitted to improve symmetry 46 is restricted to a preset amount.

- 9. A method according to claim 1, in which said SCB 42 assigned to a subset of sinks is selected from a set of predesigned SCBs of varying capacity.
- 10. An article of manufacture in computer readable form which encodes a set of instructions for performing a method according to claim 1.